REMARKS

Claims 35-37 and claims 51-63 are currently pending in the present application. Claims 58 and 61 have been amended to provide proper antecedent basis.

35 U.S.C. §102

The Examiner rejected claims 35-37 and 54-62 under 35 U.S.C. §102(e)/(a) as being anticipated by Singh. The Examiner has not presented a *prima facie* case of anticipation with regard to claims 35-37 and 54-62. According to M.P.E.P. § 706.02, in order to be anticipating under §102, the reference must teach every aspect of the claimed invention.

The Examiner relies on the structure illustrated in Figs. 1 and 2 of Singh in order to reject claims 35-37 and 54-62. Regarding independent claim 35, the Examiner has not shown that Singh teaches each and every aspect of the claimed invention. For example, the Examiner has not shown that Singh teaches forming a second contact in the well in a well in spaced relation to a first type transistor. As illustrated in Fig. 1, Singh teaches forming a second contact 36 directly in contact with the source 34 of the transistor formed in the n-well 28. As the Examiner concedes, Singh teaches "directly coupling the second contact 36 to the first source 34." Thus, Singh does not teach each and every aspect of independent claim 35. Claims 36, 37, and 51-62 depend from claim 35. Therefore, claims 35-37 and 54-62 are patentable over the cited and applied prior art.

Regarding dependent claim 36, the Examiner has not shown that Singh teaches forming a first contact a first distance from a first source, wherein the first distance defines a first component of a parasitic resistance of a well, and forming a second contact a second distance from a first source, wherein the second distance defines a second component of a parasitic resistance of a well. Singh does not teach or suggest that the parasitic resistance of the well has a first and second component. Instead, Singh teaches that the resistance of the well Rw is the resistance of the n-well region 28 between voltage $V_{DD}$ and $P^+$ region 32 (Col. 5, lines 15-17). Additionally, as discussed above, the second contact 36 is not formed a second distance from the source 34 because the second contact 36 is in direct contact with the source 36 of Singh. Thus, Singh does not teach each and every aspect of claim 36.

Further, regarding dependent claim 54, the Examiner has not shown that Singh teaches a first source coupled to a first voltage input through a series combination of first and second

components of a parasitic resistance of a well. Singh teaches that the source is coupled to voltage $V_{DD}$ through the resistance Rw of the well. Nowhere does Singh teach or suggest that the Rw has more than one component. The Examiner states that Rw = Rw' + Rw". However, Singh does not teach that Rw is made of a series resistance. Instead, Singh specifically states that Rw is the resistance of the n-well region 28 between voltage $V_{DD}$ and $P^+$ region 32 (Col. 5, lines 15-17). Thus, Singh does not teach each and every aspect of claim 54.

35 U.S.C. §103

The Examiner rejected claims 51-52 and 63 under 35 U.S.C. §103(a) as being unpatentable over Singh in view of Canaris. The Examiner has not presented a *prima facie* case of obviousness. According to the MPEP §706.02(j), to meet a threshold showing of *prima facie* obviousness, the Examiner must make three showings. The showings are: that there is some suggestion or motivation to modify the references; that there is a reasonable expectation of success; and that the prior art references teach or suggest all of the claimed limitations.

Claims 51-52 depend from independent claim 35. As discussed above, Singh does not teach or suggest every aspect of the independent claim 35. Additionally, there is no suggestion or motivation to modify Singh with Canaris as the Examiner suggests. The Examiner uses Canaris to teach coupling a first source to a second contact by forming an interconnect layer over a semiconductor. However, the second contact 36 of Singh is in direct contact with the source region 34 as illustrated in Fig. 1. Thus, there would be no motivation to modify Singh by connecting the second contact 36 to the source 34 by an interconnect layer over the semiconductor because the second contact 36 is already connected to the source 34. Thus, there is no suggestion or motivation to modify Singh as the Examiner suggests because it would only add an additional processing step.

Similarly regarding independent claim 63, the Examiner has not shown that there is a suggestion or motivation to modify Singh with Canaris for the reasons discussed above. Additionally, neither Singh nor Canaris teaches each and every aspect of the claimed invention. As discussed above, Singh does not teach not teach "forming a second contact in the well in spaced relation to the first type transistor; coupling the first contact to a first voltage input; and coupling the second contact to the first source" as claimed. Similarly, Canaris does not teach this aspect. Instead, Canaris teaches coupling Vss to the source 22 and to a **guard ring** 40 that

surrounds the transistor in the p-well 18 (Col. 3, lines 34-37 and lines 55-64). The guard ring is shown in Figs. 3 and 4A. Thus, the guard ring 40 is not a first and second contact as the Examiner suggests. Instead, guard ring 40 is a circular area around the transistor. Vss (ground) is coupled to the guard ring 40 and to the source 22 (Col. 3, lines 34-37). Therefore claims 51-52 and 63 are patentable over the cited and applied prior art.

App. Ser. No. 09/740,174
Atty. Dkt. No. MIO 0042 V2

CONCLUSION

Applicants respectfully submit that, in view of the above amendments and remarks, the application is now in condition for allowance. The Examiner is encouraged to contact the undersigned to resolve efficiently any formal matters or to discuss any aspects of the application or of this response. Otherwise, early notification of allowable subject matter is respectfully solicited.

Respectfully submitted,
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